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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/594,542	09/27/2006	Hideki Agari	2271/76931	3779

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COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

EXAMINER	
BUDD, PAUL A	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/594,542	AGARI ET AL.	
	Examiner	Art Unit	
	PAUL A. BUDD	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-7* is/are allowed.

6)☒ Claim(s) *1,2,8,9 and 11* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. Claims **1-11** are pending in the instant application. The amendments to the specification are entered. The amendments to the claims are entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim **1, 8, 9** and **11** are rejected under 35 U.S.C. 102 (b) as being anticipated by Roberts (US Patent 5,218,222).

Regarding claim **1**, Roberts discloses a semiconductor apparatus [FIG. 2] comprising

a substrate [FIG. 3; 34 & 33] with a pad [FIG. 2; 11];

an internal circuitry region [FIG. 2; 26; pull down transistors], and

a protection resistance [FIG. 2; 12; column 4 lines 26-27] formed on the substrate [FIG. 3; 34 & 33], the pad [11] being connected to a first electrode [the extension of pad over the resistance region 12 that is in contact with square contact suds] of the protection resistance [12] by a wiring [the extension of the pad over the resistance region 12];

the internal circuitry region [26] being connected to a second electrode [the 21 metal over the resistor contact area per FIG. 3] of the protection resistance [12] by a wiring [FIG. 2; the 21 leading from the resistor to the pull down transistors 26]; and

the protection resistance [12] protecting [see paragraph *3* below; as well as inherent to the structure] the internal circuitry region [26] from electrostatic discharging [see paragraph *3* below];

wherein the pad [11] is placed between [directly in-between per FIG. 2] the protection resistance [12] and the internal circuitry region [26].

4. Roberts discloses on column 2 lines 5-10, "The basic component of the output ESD protection circuit of the present invention comprises a low resistance connected in series between an output pad and conventional active output pullup and pulldown drivers". Roberts discloses on column 4 lines 26-27 "Series resistor 12 allows for enhanced ESD protection as it provides good protection to the output pullup and pulldown transistors by attenuating the voltage waveform resulting from an ESD event".

Regarding claim **8**, Roberts discloses the semiconductor apparatus as claimed in claim **1**, wherein the protection resistance [12] is formed by an impurity diffusion layer [the polysilicon resistor of Roberts contains impurities that inherently must diffuse when subjected to thermal events]. There is no requirement that the protection resistance be formed in the substrate and therefore the doped (5 ohms) polysilicon semiconductor material anticipates the broadly claimed "impurity diffusion layer".

Regarding claim **9**, Roberts discloses the semiconductor apparatus as claimed in claim **1**, wherein a protection circuit [FIG. 1; 12 & 14] is formed by the protection resistance [12] and a protection transistor [FIG. 1; 14; pull down transistors 25-26-27-28; column 4 lines 6-12] included in the internal circuitry region [FIG.2; the output pulldown transistors marked by 26].

5. The label "protection" does not structurally distinguish itself over the pull down transistors.

Regarding claim **11**, Roberts discloses the semiconductor apparatus as claimed in claim **1**, wherein the protection resistance [12] comprises a region directly contacting *the substrate* [34 & 33]. The insulator layer 33 and the p-substrate are together "*the substrate*" as claimed above. There is nothing in claim 1 or claim 11 that excludes or forbids (such as by material compositions) elements 33 and 34 together from anticipating the claimed "*substrate".*

6. Claims **1-2** are rejected under 35 U.S.C. 102 (b) as being anticipated by Usuki Hideki (Japanese Publication number 11-220094).

Regarding claim **1**, Hideki discloses a semiconductor apparatus [FIG. 1-2] comprising:

a substrate [FIG. 2; 1] with a pad [FIG. 1-2; 10a],

an internal circuitry region [FIG. 2; to the left of the FIG.], and

a protection resistance [FIG. 1-2; 2] formed on the substrate [1], the pad [10a]

being connected to a first electrode [FIG. 2; 4] of the protection resistance [2] by a wiring [7b];

the internal circuitry region [as above] being connected to a second electrode [FIG. 2; 3] of the protection resistance [2] by a wiring [7a, 5, 6]; and

the protection resistance [2] protecting [abstract; as well as inherent to the structure] the internal circuitry region [as above] from electrostatic discharging [abstract];

wherein the pad [10a] is placed between [per FIG. 1 and FIG. 4] the protection resistance [2] and the internal circuitry region [as above].

Regarding claim **2**, Hideki discloses the semiconductor apparatus as claimed in claim **1**, wherein a distance [per FIG. 2] between the pad [10a] and the first electrode [4] and a distance between the pad [10a] and the second electrode [3] are substantially the same [per FIG. 2 they are equal].

Allowable Subject Matter

7. Claims **3-7** are allowed. Claim **10** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. The applicant's traversal of the Robert's rejection of claim **1** is not convincing because the applicants arguments are not commensurate with the claim language. The applicant states, "As shown in Figs. 3-6 of Roberts which show various composite cross-sectional views, the series resistor 12 is *NOT* formed on or in substrate 34. For example, the cross-sectional view of Fig. 3 shows that insulating layer 33 is interposed between the substrate 34 and the series resistor 12". Firstly, Claim **1** recites "a protection resistance formed on the substrate". There is no claim language such as "on or IN substrate" but simply "formed on the substrate". It is well known in patent law that if element X is ON element Y there is no inherent requirement that element X be contained inside of, or be within, or even be a part of element Y. The common sense meaning of the word ON allows two separate and distinct elements to be adjacent but not contained within each other such as "the chair is on the floor". The chair need not be fabricated inside of the floor and be attached permanently to the floor if "the chair is on the floor". Additionally, any common sense usage of the word ON allows the presence of additional elements between the chair and the floor (or the p-substrate and the resistor such as the insulator layer 33 of Roberts). Common sense usage of the word ON allows the presence of a rug between the chair and the floor where both the chair and the rug are both "on the floor". This same common sense usage of the word ON applies to patent law. For this reason the applicant's traversal of the Robert's rejection is not convincing. The protection resistance of Roberts is "on the substrate" for the reasons stated above. The above position and interpretation by the Office is not new

and was stated in the Office Action dated 12 March 2009, that "There is no requirement that the protection resistance be formed in the substrate" [page 4-5].

9. The applicant's the traversal of claim **1** of the Usuki Hideki (Japanese Publication number 11-220094) rejection is not convincing because the applicants arguments are not commensurate with the claim language. All of the Office's arguments above regarding maintaining the Roberts's rejection applies to the Office's traversal of the applicant's arguments against the Usuki Hideki rejection. The meaning of the word "ON" as explained above in paragraph 8 is applied to the Usuki Hideki rejection where the resistor of Usuki Hideki is on the substrate as seen in FIG. 3. The applicants arguments that "However, the polysilicon layer 2 is *NOT* formed on substrate 1 of Usuki, and instead is stratified above, but *NOT* on, the substrate 1, as shown in Fig. 3 of Usuki" is not convincing for the reasons stated in paragraphs *8-9*.

10. The Office agrees that the applicant's amendments to claim **3** avoids the Bohm reference for the reasons stated by the applicant.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Budd whose telephone number 571-272-8796. The examiner can normally be reached on Monday to Friday 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Paul Budd/

/Jerome Jackson Jr./

Primary Examiner, Art Unit 2815